A 2.2μW 15b Incremental Delta-Sigma ADC with Output-Driven Input Segmentation

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Abstract

A micro-power incremental delta-sigma (I-ΔΣ) ADC is presented. This ADC uses its decimation filter's output to estimate the input signal level and dynamically adjusts the modulator feedback voltage, thereby reducing the integrator input range and power. For further power saving, integrator time-multiplexing is also employed. Fabricated in 0.18μm CMOS, the 0.12mm^2 ADC consumes 2.16μW at a conversion speed of 85S/s, 15.3b resolution and -2/1.5LSB INL.

Keywords: incremental delta-sigma ADC, integrator multiplexing, dual-feedback ΔΣ modulator, low power ADC

I. Introduction

Battery/wireless powered devices like bio-implant or disposable sensor are presenting increasing demands low power and energy efficient ADCs. For low frequency signal conversion, incremental delta-sigma (I-ΔΣ) ADC stands out for its tolerance to device imperfections and high resolution, while its energy efficiency is poor [1]. Attempts have been made to optimize the power consumption of the amplifier by using techniques like class-AB topology or replacing the amplifier with an inverter [2], but the long conversion time limits the energy efficiency. Higher-order loop-filter or multi-bit quantizer shorten the conversion time, but result in linearity and stability issues [1]. Two-step topology, like extended counting [3] or zoom ADC [4], has higher energy efficiency since the power and conversion time of the fine ΔΣ modulator (DSM) are relaxed using a coarse converter. However, to achieve the full ADC precision, elaborate calibration for the coarse converter as in [3] is essential. Moreover, the gain mismatch in the fine and coarse converter could result in missing code or over-ranging issues [4]. Meanwhile, the Nyquist-rate quantizer makes them prone to out-of-band noise. In this work, an output-driven input segmentation I-ΔΣ ADC is proposed, which takes advantage of two-step ADCs for improved energy efficiency while requiring no Nyquist-rate converter and does not need accurate matching between coarse/fine conversions.

III. Output-driven Input Segmentation

Fig.1 shows the proposed DSM which exploits both the quantizer output bitstream 'bs' and the digital filter output D_M to determine the modulator feedback voltage V_{FB}. Because the I-ΔΣ modulator resolution depends on the decimated number of clock periods N_{CLK} per conversion, in this scheme, after starting a conversion, the DSM first operates for a few clock periods as a coarse converter to locate the input subrange and adjusts V_{FB} to approach V_{IN} via the capacitive DAC (cap-DAC) like [4]. Meanwhile, the decimated code D_M is registered and the modulator, digital filter are reset. Above segmentation cycle can be repeated to progressively adjust V_{FB} until D_M becomes thermal noise limited. As a result, different from [4], the integrator input range and power is reduced without using a preceding SAR ADC that is sensitive to out-of-band noise.

In CMOS, a cap-DAC with 7b accuracy can be guaranteed, which sets the upper limit of the total coarse bits $\sum_{n=1}^{M} D_n \leq 7$. After M cycles of input segmentation, a D_F-bit fine ΔΣ conversion is performed and the final ADC output D_o is obtained by combining D_F and the weighted coarse codes. Because D_M and D_F are resolved from the same circuitry, errors caused by the gain mismatch between the coarse and fine converter in a general two-step ADC is absent. Moreover, only ΔΣ modulator which can tolerate large capacitor mismatch is used to perform the conversion, calibration is avoided.

The proposed ADC consists of a 2nd-order loop filter, a 1-bit quantizer, a N_{DAC}-bit cap-DAC, a digital filter and controller. Fig.2 depicts the simplified modulator diagram, where the loop filter is a switched-capacitor lossless direct integrator, which enables using only one integrator with time-multiplexing to achieve a 2nd-order noise-shaping. As a result, amplifier offset and 1/f noise cancellation techniques like auto-zero and CDS cannot be applied as an extra clock phase is required. Instead, a low frequency chopping (F_S/16) is used and the influence of chopper switches' charge-injection is minimized by changing the chopper states slightly before signal integration.

IV. Implementation

As shown in Fig.2, 3 conversions are used to achieve a reduced number of clock cycles while introducing minimal control overhead, improving the overall DSM energy efficiency. During operation, the global reset signal 'sta' clears all the memory elements before each conversion. Then, the converter resolves 3b, 4+1.5b and 8+1.5b sequentially to achieve the final 15b resolution, where the extra 1.5b is for the ±1LSB guard band to accommodate the INL induced transition error. Due to such signal segmentation, the modulator input range is ±1.5V_{LSBb} (±16.5mV with 1.4V reference) in the fine ΔΣ cycle.

The DSM with integrator time-multiplexing is shown in Fig.3. In the sampling phase S_1 of the 1st-stage, the amplifier A_1 is connected to the 2nd-stage for signal integration, and vice versa. A_1 show in Fig.4 is a gain-enhanced current mirror amplifier with input voltage modulation and output current demodulation. It consumes 1.5μA during clock phase S_2 and reduces to 0.5μA during S_1. The degradation in the modulator SQNR due to current transitions is minimized as most of the nodes of A_1 are of low impedance. The sampling capacitors C_{S1}, C_{S2} have 7 coarse units and 16 fine units (in total 7b) for V_{FB} generation. Since mismatch in the cap-DAC degrades output linearity, data weighted averaging is used for C_{S1} while mismatch in C_{S2} is 1st-order noise-shaped.

V. Experimental Results

The 0.12mm^2 prototype fabricated in a standard 0.18μm 1P6M CMOS process is shown in Fig.7. The 1.4V reference and 25.6 kHz clock are off chip and the digital filter and controller are implemented in FPGA. The ADC draws 1.2μA from a 1.8V supply. Fig.5 is the measured output spectrum of the ΔΣ

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modulator with a -3.5dB$_{FS}$ input, which validates the 2nd-order noise-shaping using only one integrator. The designed ADC has an input-referred noise of 15.8μV$_{rms}$ (42.7Hz bandwidth). The measured INL of the ADC is -2/1.5LSB (Fig.6) and Fig.7 depicts the effective resolution with different decimated clock cycles using DC histogram testing. Various precision incremental ADCs are summarized in Fig.8. The reported low power ADC is among the most energy-efficient designs, making it suitable for use in power and energy constrained systems. Moreover, as the proposed design consists only over-sampling ΔΣ modulator, errors caused by gain mismatch between coarse and fine converter, noise-folding and/or calibration issues in typical two-step ADCs are avoided.

References

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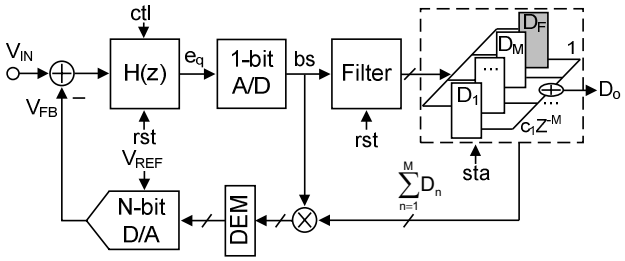

Fig.1 The proposed I-ΔΣ ADC with output-driven input segmentation

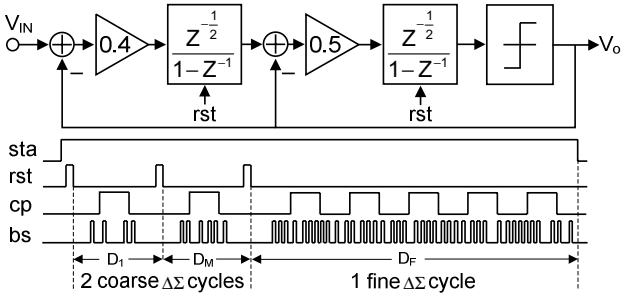

Fig.2 Block diagram and overall timing diagram of the ΔΣ modulator

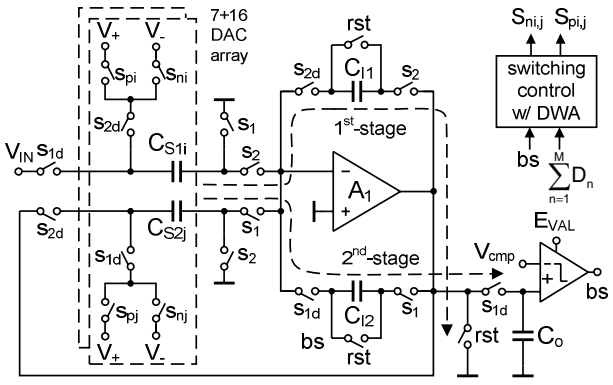

Fig.3 2nd-order ΔΣ modulator with integrator time-multiplexing

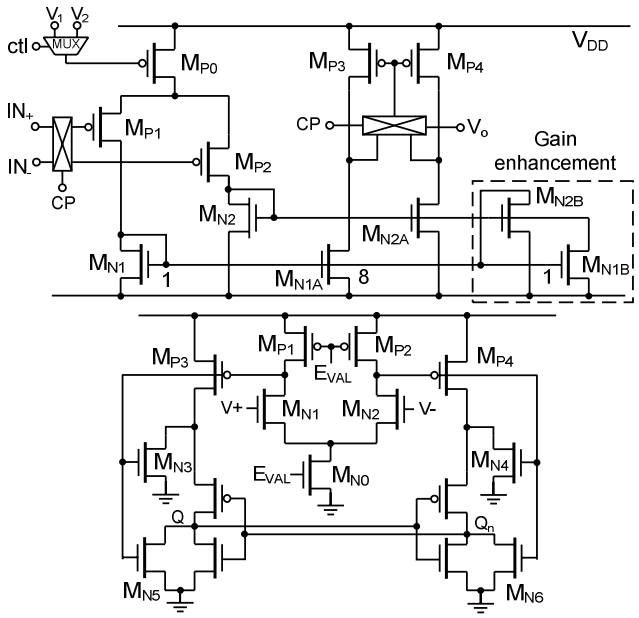

Fig.4 Schematic of the chopped amplifier with dynamic biasing and the double latch comparator

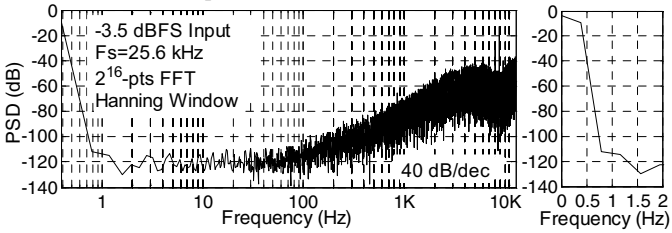

Fig.5 Measured output power spectrum with its low frequency details.

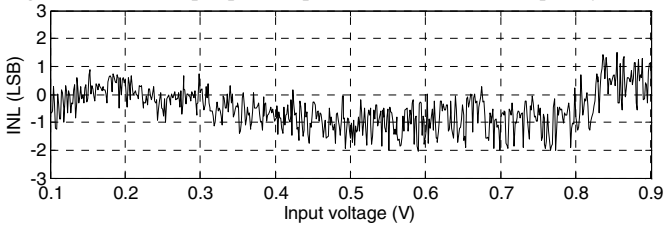

Fig.6 Measured INL as a function of input voltage

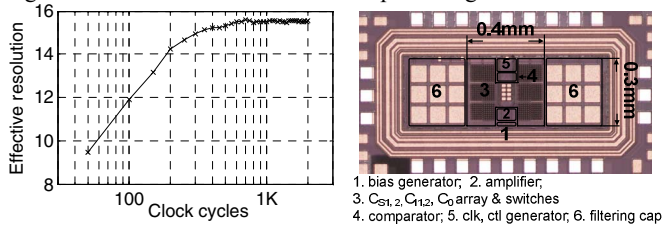

Fig.7 Effective resolution as a function of N_{clk} and the chip photo

Parameter	This work	[2] ISSCC 13	[3] JSSC 10	[4] JSSC 13
Topology	ΔΣ	ΔΣ	ΔΣ, SAR	SAR, ΔΣ
Process	0.18μm	0.16μm	0.18μm	0.16μm
Chip area	0.12mm^2	0.45mm^2	3.5mm^2	0.37mm^2
Supply	1.8V	1V	1.8V	1.8V
Power	2.16μW	20μW	38.1mW	6.3μA
$T_{conv.}$	11.7ms	<0.75ms	1μs	40ms
Input range	0.8V	0.7V	2V	1.8V
[a]SNR_{max}	85dB	81.9dB	86.3dB	119.8dB
INL (LSB)	-2/1.5 @15b	-0.6/0.4 @14b	±1 @14b	±6.3 @20b
[c]FoM_s	158dB	157.1dB	161.3dB	182.7dB

[a]SNR_{max}=20*log [Input range / (2√2*Input-referred noise)];
[c]FOM_s=SNR_{max}+10*log [1/(power*$T_{conv.}$*2)];

Fig.8 Performance summary and comparison with other I-ΔΣ ADCs